

CLAIMS:

1. A field effect transistor comprising:
 - a semiconductive layer configured to form a channel region;
 - a pair of spaced conductively doped semiconductive regions in electrical connection with the channel region of the semiconductive layer;
 - a gate intermediate the semiconductive regions; and
 - a gate dielectric layer intermediate the semiconductive layer and the gate, the gate dielectric layer being configured to align the gate with the channel region of the semiconductive layer.
2. The field effect transistor according to claim 1 wherein the semiconductive layer comprises a thin film semiconductive layer.
3. The field effect transistor according to claim 1 wherein the gate dielectric layer has a uniform thickness.
4. The field effect transistor according to claim 1 wherein the semiconductive regions are formed over the semiconductive layer.
5. The field effect transistor according to claim 1 wherein the semiconductive regions individually comprise one of a source region and a drain region, and the drain region comprises a field emitter.

1 6. The field effect transistor according to claim 5 wherein the
2 gate is provided about the field emitter.

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4 7. The field effect transistor according to claim 1 wherein the
5 semiconductive regions individually comprise one of a source region and
6 a drain region, and the drain region comprises a plurality of field
7 emitters.

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9 8. The field effect transistor according to claim 1 further
10 comprising an insulative substrate, and the semiconductive layer is
11 formed over the insulative substrate.

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13 9. The field effect transistor according to claim 8 further
14 comprising a conductive layer intermediate the insulative substrate and
15 the semiconductive layer.

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17 10. The field effect transistor according to claim 1 wherein the
18 gate has an upper outermost surface, and the gate dielectric layer has
19 an upper outermost surface substantially elevationally coincident with the
20 gate upper outermost surface.

1 11. The field effect transistor according to claim 10 wherein the
2 gate has an upper outermost surface, and the semiconductive regions
3 individually have an upper outermost surface substantially elevationally
4 coincident with the gate upper outermost surface.

5
6 12. A field emission apparatus comprising:

7 a thin film semiconductive layer;

8 a pair of spaced conductively doped semiconductive regions in
9 electrical connection with the thin film semiconductive layer, at least one
10 semiconductive region comprises a field emitter;

11 a gate intermediate the semiconductive regions; and

12 a gate dielectric layer intermediate the thin film semiconductive
13 layer and the gate.

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15 13. The field emission apparatus according to claim 12 wherein
16 the gate is formed about the field emitter.

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18 14. The field emission apparatus according to claim 12 wherein
19 the gate is configured to control current flow intermediate the
20 semiconductive regions and the emission of electrons from the field
21 emitter.

1 15. The field emission apparatus according to claim 12 wherein
2 the semiconductive regions individually comprise one of a source region
3 and a drain region over the thin film semiconductive layer.
4

5 16. The field emission apparatus according to claim 12 wherein
6 the thin film semiconductive layer forms a channel region and the gate
7 dielectric layer is configured to align the gate relative to the channel
8 region.
9

10 17. The field emission apparatus according to claim 12 wherein
11 the gate has an upper outermost surface, and the gate dielectric layer
12 has an upper outermost surface substantially elevationally coincident with
13 the gate upper outermost surface.
14

15 18. A field effect transistor comprising:
16 source and drain regions having a channel region positioned
17 therebetween;

18 a gate positioned operatively proximate the channel region, the
19 gate having an upper outermost surface; and

20 a gate dielectric layer received intermediate the channel region
21 and the gate, the gate dielectric layer having an upper outermost
22 surface substantially elevationally coincident with the gate upper
23 outermost surface.
24

1 19. The field effect transistor according to claim 18 further
2 comprising a thin film semiconductive layer intermediate the source and
3 drain regions and configured to form the channel region.

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5 20. The field effect transistor according to claim 19 wherein the
6 source and drain regions are formed over the thin film semiconductive
7 layer.

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9 21. The field effect transistor according to claim 18 wherein the
10 gate dielectric layer is configured to align the gate with the channel
11 region.

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13 22. The field effect transistor according to claim 18 wherein one
14 of the source and drain regions comprises a field emitter.

15
16 23. The field effect transistor according to claim 22 wherein the
17 gate is formed about the field emitter.

18
19 24. The field effect transistor according to claim 18 wherein one
20 of the source and drain regions comprises a plurality of field emitters.

1 25. A thin film transistor comprising:
2 a thin film semiconductive layer;
3 a pair of spaced conductively doped semiconductive regions in
4 electrical connection with the thin film semiconductive layer;
5 a self-aligned gate intermediate the semiconductive regions; and
6 a gate dielectric layer intermediate the thin film semiconductive
7 layer and the gate.

8
9 26. The thin film transistor according to claim 25 wherein the
10 semiconductive regions individually comprise one of a source region and
11 a drain region, and the drain region comprises a field emitter.

12
13 27. The thin film transistor according to claim 25 wherein the
14 gate has an upper outermost surface, and the gate dielectric layer has
15 an upper outermost surface substantially elevationally coincident with the
16 gate upper outermost surface.

1 28. A field emission apparatus comprising:
2 an insulative substrate;
3 a conductive layer over the insulative substrate;
4 a thin film semiconductive layer over the insulative substrate and
5 the conductive layer;
6 a plurality of semiconductive regions formed over and in electrical
7 connection with the thin film semiconductive layer, the semiconductive
8 regions individually including one of a source region and drain region,
9 the drain region being formed as a field emitter and the thin film
10 semiconductive layer comprising a channel region intermediate the source
11 region and the drain region, the source region and drain region
12 individually include an upper outermost surface;
13 a gate positioned operatively proximate and self-aligned relative to
14 the channel region, the gate being provided about the field emitter and
15 having an upper outermost surface;
16 a gate dielectric layer intermediate the gate and the thin film
17 semiconductive layer, the gate dielectric layer having an upper outermost
18 surface substantially elevationally coincident with the source region upper
19 outermost surface, drain region upper outermost surface and gate upper
20 outermost surface, the gate dielectric layer further having a uniform
21 thickness to align the gate relative to the channel region; and
22 a plurality of conductors individually coupled with one of the gate,
23 the drain region and the source region.
24

1 29. A method of forming a field effect transistor comprising:
2 forming a semiconductive layer having a channel region;
3 forming plural spaced conductively doped semiconductive regions
4 electrically coupled with the semiconductive layer;
5 forming a gate dielectric layer over the semiconductive layer;
6 forming a gate over the gate dielectric layer; and
7 aligning the gate with the channel region using the gate dielectric
8 layer.

9
10 30. The method according to claim 29 wherein the forming the
11 semiconductive layer comprises forming a thin film semiconductive layer.

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13 31. The method according to claim 29 wherein the forming and
14 the aligning of the gate comprise forming a gate layer over the gate
15 dielectric layer and removing portions of the gate dielectric layer and
16 the gate layer.

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18 32. The method according to claim 31 wherein the removing
19 portions of the gate dielectric layer and the gate layer occur in a
20 common processing step.

21
22 33. The method according to claim 31 wherein the removing
23 comprises chemical-mechanical polishing.
24

1 34. The method according to claim 31 wherein the removing
2 comprises initially removing respective uppermost surfaces of the
3 semiconductive regions before removing any gate material above the
4 gate.

5
6 35. The method according to claim 31 wherein the removing
7 provides the gate dielectric layer with an upper outermost surface
8 substantially elevationally coincident with an upper outermost surface of
9 the gate.

10
11 36. The method according to claim 29 wherein the forming the
12 gate comprises forming without using any mask.

13
14 37. The method according to claim 29 wherein the forming the
15 gate comprises depositing gate material over the gate dielectric layer,
16 and removing portions of the gate material without using a mask over
17 the gate during the removing.

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19 38. The method according to claim 29 wherein the forming the
20 semiconductive regions comprises forming source and drain regions over
21 the semiconductive layer.

1 39. The method according to claim 29 wherein the forming the
2 semiconductive regions comprises forming a drain region comprising a
3 field emitter.

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5 40. The method according to claim 29 wherein the forming the
6 semiconductive regions comprises forming a drain region comprising a
7 plurality of field emitters.

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9 41. A method of forming a field effect transistor comprising:
10 providing a semiconductive layer;
11 forming plural semiconductive regions electrically coupled with the
12 semiconductive layer;
13 forming a gate dielectric layer over the semiconductive layer; and
14 forming a gate of gate material over the gate dielectric layer
15 without the use of a mask over the gate material.

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17 42. The method according to claim 41 further comprising
18 aligning the gate with a channel region within the semiconductive layer
19 using the gate dielectric layer.

20
21 43. The method according to claim 41 wherein the providing the
22 semiconductive layer comprises forming a thin film semiconductive layer.

1 44. The method according to claim 41 wherein the forming the
2 gate comprises removing portions of the gate dielectric layer and a gate
3 layer in a common step.

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5 45. The method according to claim 44 wherein the removing
6 self-aligns the gate with a channel region within the semiconductive
7 layer.

8
9 46. The method according to claim 44 wherein the removing
10 comprises chemical-mechanical polishing.

11
12 47. The method according to claim 44 wherein the removing
13 provides the gate dielectric layer with an upper outermost surface
14 substantially elevationally coincident with an upper outermost surface of
15 the gate.

16
17 48. The method according to claim 44 wherein the removing
18 comprises initially removing respective uppermost surfaces of the
19 semiconductive regions before removing any gate material above the
20 gate.

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22 49. The method according to claim 44 wherein the forming the
23 semiconductive regions comprises forming a drain region comprising a
24 field emitter.

1 50. The method according to claim 44 wherein the forming the
2 semiconductive regions comprises forming a drain region comprising a
3 plurality of field emitters.

4
5 51. A method of forming a field effect transistor comprising:
6 providing a semiconductive layer having a channel region;
7 providing plural semiconductive regions electrically coupled with the
8 channel region;
9 forming a gate dielectric layer over the semiconductive layer; and
10 forming a gate of gate material comprising:
11 depositing the gate material over the gate dielectric layer;
12 removing portions of the gate material without using a mask
13 over the gate during the removing.

14
15 52. The method according to claim 51 further comprising
16 aligning the gate with the channel region using the gate dielectric layer.

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18 53. The method according to claim 51 wherein the providing the
19 semiconductive layer comprises forming a thin film semiconductive layer.

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21 54. The method according to claim 51 wherein the removing
22 comprises removing portions of the gate dielectric layer and the gate
23 material in a common step.

1 55. The method according to claim 51 wherein the removing
2 comprises chemical-mechanical polishing.

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4 56. The method according to claim 51 wherein the removing
5 provides the gate dielectric layer with an upper outermost surface
6 substantially elevationally coincident with an upper outermost surface of
7 the gate.

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9 57. The method according to claim 51 wherein the removing
10 comprises initially removing respective uppermost surfaces of the
11 semiconductive regions before removing any gate material above the
12 gate.

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14 58. The method according to claim 51 wherein the providing the
15 semiconductive regions comprises forming a drain region comprising a
16 field emitter.

17
18 59. The method according to claim 51 wherein the providing the
19 semiconductive regions comprises forming a drain region comprising a
20 plurality of field emitters.

1 60. A method of forming a thin film transistor comprising:
2 forming a thin film semiconductive layer having a channel region;
3 providing plural semiconductive regions electrically coupled with the
4 channel region;
5 forming a gate dielectric layer over the thin film semiconductive
6 layer;
7 forming a gate layer over the gate dielectric layer; and
8 removing portions of the gate dielectric layer and the gate layer
9 providing a gate self-aligned with the channel region.
10

11 61. The method according to claim 60 wherein the providing the
12 semiconductive regions comprises forming a drain region comprising a
13 field emitter.
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15 62. The method according to claim 61 wherein the forming the
16 gate layer comprises forming the gate layer about the field emitter.
17

18 63. The method according to claim 60 wherein the removing
19 comprises chemical-mechanical polishing.
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21 64. The method according to claim 60 wherein the removing
22 provides the gate dielectric layer with an upper outermost surface
23 substantially elevationally coincident with an upper outermost surface of
24 the gate.

1 65. The method according to claim 60 wherein the removing
2 comprises initially removing respective uppermost surfaces of the
3 semiconductive regions before removing any gate material above the
4 gate.

5
6 66. A method of forming a thin film transistor comprising:
7 forming source and drain regions having a thin film channel
8 region positioned therebetween;

9 forming a gate layer and a gate dielectric layer over the thin film
10 channel region; and

11 polishing the gate layer to form an isolated gate intermediate the
12 source and drain regions over the thin film channel region.

13
14 67. The method according to claim 66 wherein the forming the
15 gate layer comprises forming the gate layer over the source and drain
16 regions.

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18 68. The method according to claim 66 further comprising
19 aligning the gate using the gate dielectric layer.

20
21 69. The method according to claim 66 wherein the forming the
22 source and drain regions comprises forming the drain region as a field
23 emitter.

1 70. The method according to claim 66 wherein the polishing
2 comprises chemical-mechanical polishing.
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4 71. The method according to claim 66 wherein the polishing
5 provides the gate dielectric layer with an upper outermost surface
6 substantially elevationally coincident with an upper outermost surface of
7 the gate.
8

9 72. The method according to claim 66 wherein the polishing
10 comprises polishing the gate dielectric layer.
11

12 73. The method according to claim 66 wherein the polishing
13 comprises initially polishing respective uppermost surfaces of the source
14 and drain regions before polishing any portions of the gate layer above
15 the gate.
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